Abstracts

Reduced order modeling of coupled on-chip interconnects for silicon-based RF integrated circuits

Ji Zheng, V.K. Tripathi and A. Weisshaar. "Reduced order modeling of coupled on-chip interconnects for silicon-based RF integrated circuits." 2000 MTT-S International Microwave Symposium Digest 00.2 (2000 Vol. II [MWSYM]): 973-976.

A reduced order modeling methodology of coupled on-chip interconnects for silicon-based RF integrated circuits is presented. The modeling approach is based on a mixed PEEC formulation combined with a hierarchical model order I reduction technique and captures both the conductor skin and proximity effects and the substrate skin effect. The response of the CAD-oriented macromodel is in good agreement with EM simulation results.

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